

REMARKS

Claims 1-46 are pending in this application. Claims 47-64 are withdrawn. Claim 5 has been amended herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

Claim 5 was objected to because of informalities. However, claim 5 has been amended such that this objection is now moot.

Claims 1-46 were rejected under 35 U.S.C. 102(b) as being anticipated by Hara, *et al.* The applicant respectfully disagrees. More specifically, in his discussion of independent claim 1, the Examiner states that "Figures 1-13D discloses a first scribe line having a selected width extending along a first direction and adjacent a first die of the multiplicity of dies (Figure 4); a second scribe line having a selected width extending along a second direction adjacent the first die and intersecting the first scribe line at a corner point of the first die; at least one free area defined on at least one of the first and second scribe lines where placement of a test key is restricted (Figures 13A-13D).

However, *none* of the figures in U.S. Patent No. 5,371,411 to Hara, *et al.* even show a scribe line. Likewise, the term "scribe line" is not even suggested or mentioned in the Hara, *et al.* specification, much less disclosed or discussed. It appears that the Examiner has erroneously considered the slots 13 of the Hara, *et al.* reference as "scribe lines".

Further, the present independent claims clearly require a wafer that includes a multiplicity of dies (semiconductor chips) before separation or singulation. The Hara, *et al.* reference discloses the use of a guard ring with slots *after* separation or singulation.

Claim 1 also requires a "free area" to be defined on, or as part of, a scribe line (preferably at the intersection of two scribe lines) where test keys may not be placed. Nothing in Hara, *et al.* even suggests much less teaches such free areas. Test keys 18 are shown on the wafer 10 of FIG. 1, and are shown on the scribe lines between two adjacent semiconductor chips or dies prior to singulation in FIGs. 3A-4, FIG. 7, and FIGs. 9-10C. Of course, the Hara, *et al.* reference cannot include "free areas", as discussed and taught by the present invention, since the "free areas" would be on the scribe lines that are cut or severed away during the separation or singulation process. Likewise, the Hara, *et al.* reference cannot include "test keys" as discussed and taught by the present invention since the "test keys" are also located on the wafer scribe lines and will not exist after singulation or separation.

To qualify as a 102(b) reference, *every* element of a claim must be disclosed in the reference. *None (not one)* of the elements of claim 1 are even disclosed (much less taught) in the Hara, *et al.* reference. The only thing in common to claim 1 and the reference is a semiconductor device or die. Even so, the claims refer to a wafer defining a *multiplicity* of dies or devices, whereas Hara, *et al.* discloses a slotted guard ring around a *single* die or device.

Claims 2-32 depend directly or indirectly from claim 1 and are therefore allowable for the reasons discussed above as well as for each of the additional limitations included in these dependent claims.

As was discussed above, in the rejection of claim 1, the Examiner erroneously equates the scribe lines of the present invention with the guard ring 12 of the reference. However, in claim 9 the Examiner has erroneously equated the slots 13 in the guard ring 12 with the test keys 18 of the present invention.

Independent claim 33 was also rejected under 35 U.S.C. 102(b) as being anticipated by Hara, *et al.* However, claim 33 includes every limitation of claim 1, as well as further requiring additional scribe lines and free areas. Therefore, since Hara, *et al.* does not even mention or such, much less teach, scribe lines or test keys, independent claim 33 is allowable for the reasons discussed above with respect to claim 1 as well as for the additional limitations.

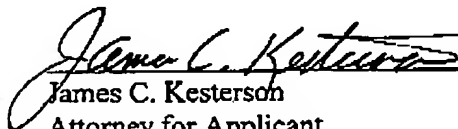
Dependent claims 34-46 are therefore allowable for depending from a claim deemed allowable, as well as for their own additional limitations.

Applicant has made amendments to paragraph 0066 to correct typographical errors.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge the appropriate fees to Deposit Account No. 50-1065.

Respectfully submitted,

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Date


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